I. AMENDMENT

In the Claims:

Listed below is a listing of pending claims. This listing of claims will replace all prior versions, and listings, of claims for the present application:

Claims 1-5 (Canceled).

6. (Currently Amended) A semiconductor device formed using a photo-definable layer in a positive mask scheme, comprising:

a substrate;

at least one feature formed on said substrate by converting selected portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation in a positive mask scheme and by using non-exposed portions of said photo-definable layer as a mask to form said at least one feature; and

an insulative layer formed on said substrate from said non-exposed portions of said photo-definable layer which (1) remain after the positive mask scheme completes all masking steps that form the at least one feature and (2) are then subsequently converted to the insulative layer through exposure to further electro-magnetic radiation.

7. (Canceled).

8. (Previously Presented) The semiconductor device of claim 6, wherein said photo-definable layer comprises an organosilicon resist.

9. (Original) The semiconductor device of claim 8, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS).

10. (Original) The semiconductor device of claim 9, wherein said feature is part of a memory cell array.

Claims 11-18 (Canceled).

19. (Currently Amended) A patterned insulative structure within a semiconductor device formed using a photo-definable layer in a positive mask scheme, comprising:

a substrate; and

a patterned insulative layer formed on said substrate by converting selected portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation in a positive mask scheme and by using non-exposed portions of said photo-definable layer as a mask to form said patterned insulative layer wherein said insulative layer comprises an oxide layer and the non-exposed portions of said photo-definable layer are utilized to mask the oxide layer to form said patterned insulative layer~~.~~

wherein said patterned insulative layer comprises non-exposed portions of said photo-definable layer that were converted into additional insulative material after formation of said patterned insulative layer.

20. (Canceled).

21. (Previously Presented) The patterned insulative structure of claim 19, wherein said photo-definable layer comprises an organosilicon resist.

22. (Original) The patterned insulative structure of claim 21, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS).

23. (Original) The patterned insulative structure of claim 22, wherein said insulative layer comprises a plurality of trench structures within a memory cell array.

Claims 24-33 (Canceled).

34. (Currently Amended) A conductive interconnect structure within a semiconductor device formed using a photo-definable layer, comprising:

a substrate;

a first conductive layer over said substrate;

an insulative layer over said conductive layer; and

a second conductive layer formed within a desired portion of said insulative layer to create a conductive interconnect structure connected to said first conductive layer, said second conductive layer being formed within the desired portion of said insulative layer, said desired portion of said insulative layer being a void formed by converting selected portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation in a positive mask scheme, by using non-exposed portions of said photo-definable layer as a mask to form a pattern within said insulative layer, and by using non-exposed portions of said photo-definable layer as a sacrificial mask in etching said ~~second~~ first conductive layer.

35. (Original) The conductive interconnect structure of claim 34, wherein said photo-definable layer comprises an organosilicon resist.

36. (Original) The conductive interconnect structure of claim 35, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS).

37. (Original) The conductive interconnect structure of claim 34, wherein said substrate includes a plurality of transistor gate structures for a memory cell array.

Claims 38-48 (Canceled).

49. (Currently Amended) A patterned insulative structure within a semiconductor device using a photo-definable layer as a mask layer, comprising:

a substrate; and

an insulative layer on said substrate formed by covering a photo-definable layer with a separate patterned organic photoresist, by converting unmasked portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation in a positive mask scheme, and by using non-exposed portions of said photo-definable layer and said organic photoresist as a mask to form a pattern within said insulative layer~~.~~

wherein said insulative layer comprises non-exposed portions of said photo-definable layer subsequently converted into additional insulative material.

50. (Original) The patterned insulative structure of claim 49, wherein said photo-definable layer comprises an organosilicon resist.

51. (Original) The patterned oxide structure of claim 50, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS).

52. (Original) The patterned insulative structure of claim 51, wherein said insulative layer comprises an oxide layer.

53. (Original) The patterned insulative structure of claim 52, wherein said insulative layer comprises a plurality of trench structures within a memory cell array.

Claims 54-100 (Canceled).

RESPONSE TO NOTICE OF NON-COMPLIANT AMENDMENT

Claim 19 has been corrected to correct the status identifier. Claims 6, 8-10, 19, 21-23, 34-37 and 49-53 are pending in the present application.

No extension of time is believed to be needed in connection with the filing of this paper. However, if an extension is deemed to be needed, please consider this paper to be a request for such extension and deduct any required fee from deposit account 10-1205/MTIP:003D1. Should any fees under 37 CRF 1.16-1.21 be required for any other reason relating to the enclosed materials, the Commissioner is authorized to deduct such fees from Deposit Account No. 10-1205/MTIP:003D1. The examiner is invited to contact the undersigned at the phone number indicated below with any questions or comments, or to otherwise facilitate expeditious and compact prosecution of the application.

Respectfully submitted,

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